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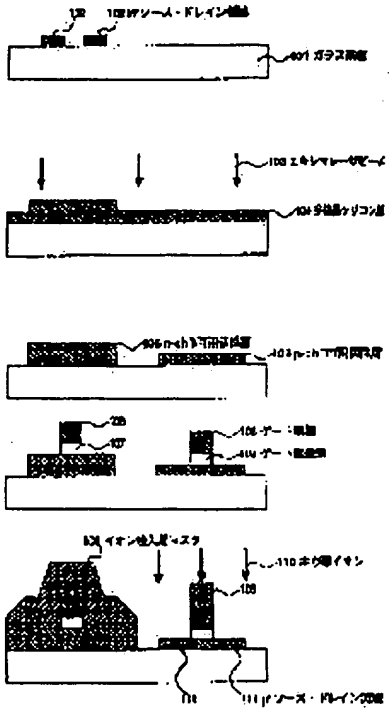
(71)Applicant : **NEC CORP**
(72)Inventor : **NAKAMURA KENICHI**

(54) CMOS THIN-FILM TRANSISTOR AND ITS MANUFACTURE

(57)Abstract:
PURPOSE: To realize concurrently both the high withstanding voltage and high- speed operation of a CMOS thin-film circuit, by giving to its n-channel TFT a stagger structure capable of achieving a high withstanding voltage, and by giving to its p-channel TFT a planar structure capable of accomplishing a high-speed operation.
CONSTITUTION: On a glass substrate 101, n+ source and drain regions 102, 102 are formed, and then, a polycrystal silicon film 104 is formed. Subsequently, the polycrystal silicon film 104 is patterned, and both such an n-channel TFT active layer 105 having an island it and such a p-channel TFT active layer 106 having an island structure that the n+ source and drain regions 102, 102 convered with it and such a p-channel TFT active layer 106 having an island structure as not to overlap with the n+ source and drain regions 102, 102 are formed respectively. Then, on both the active layer 105 and the glass substrate 101, both a gate insulation film 107 and a gate electrode 108 are formed respectively. Subsequently, an ion implantation mask 109 is formed both on the gate electrode 108 present on the p-channel IFT active layer 106 and so as to cover the n-channel TFT active layer 105. Thereafter, an ion implantation is performed, and p+ source and drain regions 111, 111 are formed respectively.



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* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] CMOS TFT which can produce this invention with the few number of processes especially about CMOS TFT and its manufacture technique -- it is related with the manufacture technique to call
[0002]
[Description of the Prior Art] In connection with development of a high-advancement-in-information-technology age, the importance of an I/O device is increasing and low-cost-izing of equipment and the enhancement in a reliability are demanded. Such under the background, the research which really forms a circumference drive circuit on the same substrate as I/O devices, such as a liquid-crystal-display element (LCD) and a contact type image sensor (CIS), is performed actively. It is because a fall of the reliability by the poor contact in a connection etc. can be suppressed by drive circuit unification while the connection cost of a circumference drive circuit and a device is reducible. It is thought that CMOS circuit arrangement which are excellent in respect of power consumption or the stability of operation as the technique of constituting this drive circuit from a thin film circuit are advantageous. On the other hand, in order to reduce the cost of a device further, it is required that the number of processes is cut down and a throughput is raised. It can be said that the technique which forms CMOS circuit arrangement with the few number of processes from the above point is important.
[0003] Conventional CMOS TFT and its conventional production process are explained using drawing 5 . First, as shown in drawing 5 (a), after depositing an amorphous silicon (a-Si) layer by the LPCVD method on a glass substrate 301, annealing is performed by the solid phase grown method, the excimer laser annealing method, etc., and a polycrystal silicon (poly-Si) layer is formed. Next, patterning is carried out to island-like structure and it is n-ch. The barrier layer for TFT 302, and p-ch The barrier layer for TFT 303 is formed. Next, as shown in drawing 5 (b), it is SiO2 by the LPCVD method. After depositing a layer and depositing the n+poly-Si layer which contains Lynn in high concentration by the LPCVD method further, patterning is performed and the gate insulator layer 304 and the gate electrode 305 are formed. Next, as shown in drawing 5 (c), after applying a resist, patterning is performed, and it is p-ch. After forming the mask for the 1st ion implantation 306 on the barrier layer for TFT 303, the phosphorus ion 307 is poured in with ion-implantation, and it is n-ch. n+ source drain field 308 which contains Lynn in high concentration is formed in a part of barrier layer for TFT. Next, as shown in drawing 6 (a), after removing the mask for the 1st ion implantation 306, a resist is applied and patterning is performed, and it is p-ch. The gate electrode 305 top on TFT barrier layer, and n-ch The barrier layer for TFT 302, and n+ The mask for the 2nd ion implantation 309 is formed so that the source drain field 308 may be covered. Next, the boron ion 310 is poured in with ion-implantation, and it is p-ch. p+ source drain field 311 which contains boron in high concentration is formed in a part of barrier layer for TFT 303. Next, a contact hole is formed, after removing the mask for the 2nd ion implantation 309 and forming the layer insulation layer 312, as shown in drawing 6 (b). Furthermore, after depositing an aluminum layer by the spatter, patterning is performed and the source drain electrode 313 is formed.
[0004]
[Problem(s) to be Solved by the Invention] Generally, it is n-ch. TFT is p-ch. Compared with TFT, pressure-proofing is low. For this reason, pressure-proofing of CMOS thin film circuit is n-ch. Since it will be restricted by pressure-proofing of TFT, it is n-ch. A raise in pressure-proofing of TFT is important. Moreover, it is also required for highly-efficient-izing of a device that a leakage current is stopped low. poly-Si A big leakage current flows compared with MOSFET which formed TFT in bulk silicon by the electric-field emission current through the level near a ****** gap. (It reference-IEEE- -transaction- -ON- -electron- -debye-******s (IEEE Trans.ON Electron Devices).) Vol.ED-32 No.9 pp.1878 -- for the enhancement in this pressure-proofing, and a reduction of a leakage current It is effective to ease the electric field in a drain edge. Until now LDD (Lightly Doped Drain) structure (a reference Institute of Electronics and Communication Engineers synthesis national conference, 2-20, pp.271 1978) and offset structure (reference IEEE electron debye ********** ()) [IEEE] Electron Device LettersVol.EDL-8, No.9, and pp. -- although 434 and 1987 are proposed and put in practical use, the increase in a process is not avoided As a means to perform a raise in pressure-proofing, and a reduction of a leakage current by comparatively simple technique, it can consider forming TFT with order stagger structure. With order stagger structure, since the channel-table side and the source drain field front face have the structure where only the thickness of a barrier layer was separated and very small offset structure is formed, the enhancement in pressure-proofing and a reduction of a leakage current can be attained. However, with order stagger structure, in order to make the gate and a source drain field overlap, a parasitic capacitance becomes large compared with planar type TFT, and the problem

that a working speed falls compared with planar type TFT arises.
[0005] Moreover, the impurity concentration immediately after injection of the source drain field formed by the ion implantation of the conventional TFT becomes uneven in the depth orientation. Although the homogeneity of the concentration of the depth orientation is improved by diffusion when activating an impurity at the elevated temperature of about 1000 degrees C after injection, in a low-temperature process 600 degrees C or less, a diffusion coefficient is very small and the concentration of the depth orientation is hard to be equalized. The problem are easy to cause a poor contact, increase of a leakage current, etc. had the heterogeneity of the depth orientation of this impurity concentration. Compared with boron, it becomes steep, and is easy to produce heterogeneity in the depth orientation, and the concentration profile at the time of pouring in especially Lynn is n-ch. There was a problem that the enhancement in the property of TFT was difficult.
[0006] Moreover, with the conventional CMOS thin-film-circuit-fabrication technique, it is n+. A layer and p+ In order to form a layer, two ion implantations needed to be performed. For this reason, it was difficult to reduce the number of processes, and the problem that the cost reduction of a device was difficult had arisen.
[0007] The purpose of this invention can be produced with the few number of processes, and is to offer CMOS TFT in which high pressure-proofing and a fast turn around are possible, and its manufacture technique.
[0008]
[Means for Solving the Problem] n type source drain field where this invention was formed on the insulating substrate in order to solve the technical probrem mentioned above and which consists of a n-type semiconductor which contains n type impurity in high concentration, p type source drain field which consists of a p type semiconductor which contains p type impurity in high concentration, The barrier layer which consists of a semiconductor formed so that the aforementioned source drain field might be touched, The gate insulator layer formed so that the aforementioned barrier layer might be covered, and the gate electrode formed so that a part of aforementioned gate insulator layer might be covered, The layer insulation layer formed so that the aforementioned gate electrode and the aforementioned gate insulator layer might be covered, In CMOS TFT which has the n channel TFT and p-channel TFT which consist of a source drain electrode electrically connected with the aforementioned source drain field The aforementioned n channel TFT becomes the aforementioned barrier-layer lower part from the stagger structure TFT which has an island-like n-type-semiconductor layer as an n type source drain field. The aforementioned p-channel TFT offers CMOS TFT characterized by consisting of the planar-structure TFT which has the aforementioned p type source drain field formed in the same layer as the aforementioned barrier layer.
[0009] Moreover, the process which forms n type source drain field which consists of a n-type semiconductor which contains n type impurity in high concentration on an insulating substrate, The process which deposits a semiconductor layer on the aforementioned n type source drain field and an insulating substrate, The barrier layer for n channel TFT which carries out patterning of the aforementioned semiconductor layer, covers the aforementioned n type source drain field, and has island-like structure, The process which forms the barrier layer for p-channel TFT which has island-like structure on the aforementioned insulating substrate in which the aforementioned n type source drain field is not formed, The process which forms a gate insulator layer so that the aforementioned barrier layer may be covered, and the process which forms a gate electrode so that a part of aforementioned gate insulator layer may be covered, So that the process which forms p type source drain field of the aforementioned p-channel TFT in a self-matching target, and the aforementioned gate electrode and the aforementioned gate insulator layer may be covered The manufacture technique of CMOS TFT which consists of a process which forms a layer insulation layer, and a process which forms the source drain electrode electrically connected with the aforementioned source drain field is offered.
[0010]
[Example] Next, the 1st example of this invention is explained with reference to a drawing. n+ which uses a silane and a phosphoretted hydrogen by the LPCVD method on a glass substrate 101, and contains Lynn three or more [1021cm -] at 600 degrees C as first shown in drawing 1 (a) After depositing 1000A of poly-Si thin films, patterning is performed, and it is n+. The source drain field 102 is formed. Next, as shown in drawing 1 (b), after depositing 1000A of a-Si layers at 500 degrees C by the LPCVD method using a disilane, it crystallizes by irradiating the excimer laser beam 103, and the polycrystal silicon layer 104 is formed. Next, as shown in drawing 1 (c), patterning of the polycrystal silicon layer 104 is carried out, and it is n+. n-ch of the island-like structure which covers the source drain field 102 The barrier layer for TFT 105, and n+ p-ch of island-like structure which does not lap with the source drain field 102 The barrier layer for TFT 106 is formed. Next, as shown in drawing 2 (a), a silane and oxygen are used by the LPCVD method on the barrier layer 105 and the glass substrate 101, and it is SiO2 at 400 degrees C. 2000A of layers is deposited, a silane and a phosphoretted hydrogen are further used by the LPCVD method, and it is Lynn at 600 degrees C 1021cm-3 n+ contained above After depositing 1000A of layers, patterning is performed and the gate insulator layer 107 and the gate electrode 108 are formed. Next, as shown in drawing 2 (b), after applying a resist, patterning is performed, and it is p-ch. On the gate electrode 108 on the barrier layer for TFT. n-ch After forming the mask for ion implantations 109 so that the barrier layer for TFT 105 may be covered, It is the boron ion 110 by ion-implantation Acceleration voltage and 15keV dose 5x101 5 mc-2 It pours in. p-ch It is boron to the field in which the gate electrode 108 is not formed among the barrier layers for TFT 106 1021cm-3 p+ contained above The source drain field 111 is formed. Furthermore, annealing is performed in the nitrogen ambient atmosphere for 600 degree-C 24 hours, and the impurity of a source drain field is activated. Next, it is SiNX by the plasma CVD method as shown in drawing 2 (c), after removing the mask for ion implantations 109. A layer is deposited and the layer insulation layer 112 is formed. Furthermore, patterning is performed and they are the layer insulation layer 112 and n-ch. After forming a contact hole in the barrier layer for TFT 105, 3000A of aluminum is deposited by

the spatter, patterning is performed, and source drain field ****** 113 is formed.
[0011] Next, the 2nd example is explained with reference to a drawing. First, patterning is performed and a pad 202 is formed, after depositing 1000A of tungsten silicide layers by the spatter on a glass substrate 201, as shown in drawing 3 (a). Next, a silane and a phosphoretted hydrogen are used by the LPCVD method so that a pad 202 may be covered, as shown in drawing 3 (b), and it is Lynn at 600 degrees C 1021cm-3 n+ which carries out grade inclusion above After depositing 1000A of poly-Si thin films, patterning is performed, and it is n+. The source drain field 203 is formed. Next, as shown in drawing 3 (c), after depositing 1000A of a-Si layers at 500 degrees C by the LPCVD method using a disilane, it crystallizes by irradiating the excimer laser beam 204, and the poly-Si layer 205 is formed. Next, as shown in drawing 4 (a), patterning of the poly-Si layer 205 is carried out to island-like structure, and it is n+. A barrier layer 206 is formed so that the source drain field 203 may be covered. Furthermore, a silane and oxygen are used by the LPCVD method on the barrier layer 205 and the glass substrate 201, and it is SiO2 at 400 degrees C. 2000A of layers is deposited, a silane and a phosphoretted hydrogen are further used by the LPCVD method, and it is Lynn at 600 degrees C 1021cm-3 After depositing 2000A of the n+poly-Si layers contained above, patterning is performed and the gate insulator layer 207 and the gate electrode 208 are formed. Patterning is performed, after applying a resist, as shown in drawing 4 (b). Next, on the gate electrode 208, The part on a pad 202 is removed and it is n+. After forming the mask for ion implantations 209 so that the source drain field 203 may be covered, It is the boron ion 210 by ion-implantation Acceleration voltage 15keV and dose 5x101 5 cm-2 It pours in. It is boron to the field in which the gate electrode 208 and the mask for ion implantations 209 are not formed among barrier layers 206 021cm-3 p+ contained above The source drain field 211 is formed. Next, it is SiNx by the plasma CVD method as shown in drawing 4 (c), after removing the mask for ion implantations 209. 2000A of layers is deposited, the layer insulation layer 212 is formed, patterning is performed and a contact hole is formed in the layer insulation layer 212 and the barrier layer 206. Next, 3000A of aluminum is deposited by the spatter, patterning is performed, and the source drain electrode 213 is formed.
[0012] CMOS thin film circuit is [an ion implantation] producible only also as 1 time as mentioned above. At this example, it is n-ch. It is n-ch although the production process which makes TFT order stagger structure and makes p-chTFT a planar structure was described. TFT is made into a planar structure and it is p-ch. It is also possible to produce TFT as order stagger structure.
[0013] Moreover, at the 2nd example, it is p+. By forming the pad with which an etching rate becomes the source drain field lower part from a late tungsten silicide, etching at the time of contact hole formation of a source drain field can be stopped with a pad. For this reason, n+ Or p+ A source drain field and a source drain inter-electrode contact property can be raised.
[0014]
[Effect of the Invention] The TFT according to this invention as explained above is n-ch. TFT is made into the stagger structure in which a raise in pressure-proofing is possible, and it is p-ch. Since TFT is made into the accelerable planar structure, it has the effect that a raise in pressure-proofing and fast turn around of CMOS thin film circuit are simultaneously realizable.
[0015] Furthermore, n-ch Since a leakage current can be reduced by making TFT into stagger structure, it has the effect that power consumption can be reduced.
[0016] Moreover, the manufacture technique of the TFT of this invention is n-ch. Since it has the process which performs an impurity introduction of the source drain field of TFT by in-situ doping by the LPCVD method, an impurity profile becomes uniform, in order that a contact property may improve, while the yield improves, a leakage current decreases, and it has the effect that the homogeneity of TFT property in a substrate side improves further. Furthermore, it is n-ch in 1 time of an ion-implantation process. TFT and p-ch Since TFT of both the types of TFT is producible, the number of processes of CMOS thin film circuit can be cut down, and it has the characteristic feature that the cost of the I/O device which unified CMOS drive circuit can be reduced.

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* NOTICES *

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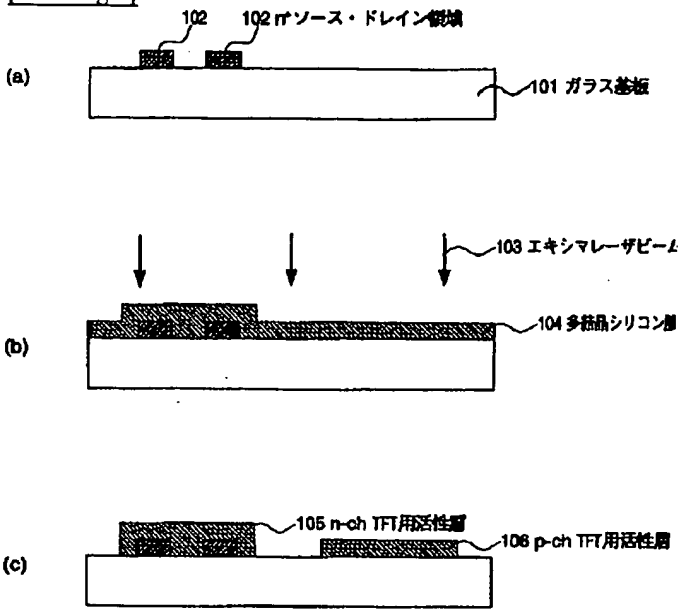
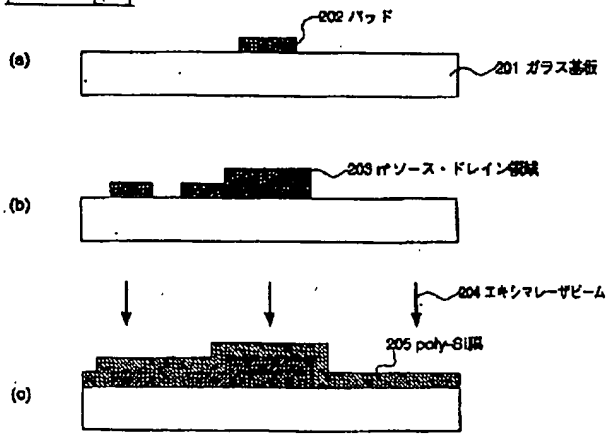
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

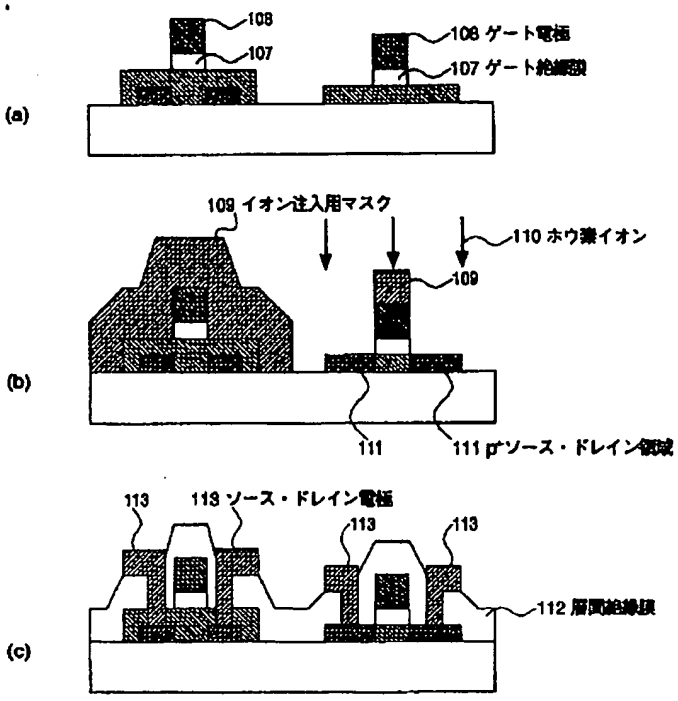
[Drawing 1]



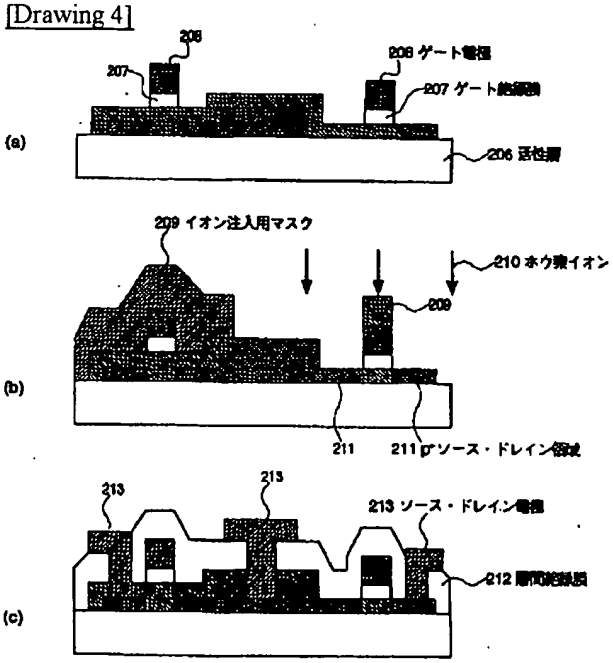
[Drawing 3]



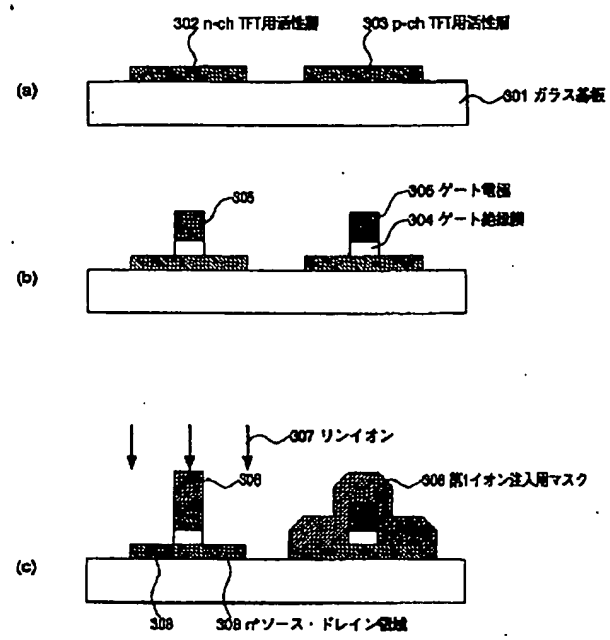
[Drawing 2]



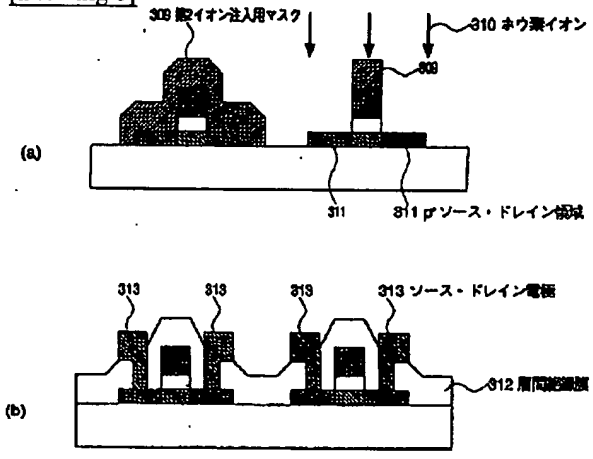
[Drawing 4]



[Drawing 5]



[Drawing 6]



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